IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl.No.:	10/779,903	Confirmation No.: 9629
Appellant:	Zhou et al	
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Docket:	TI-36355	
Cust.No.:	23494	

APPEAL BRIEF

Commissioner for Patents
P.O.Box 1450
Alexandria VA 22313-1450

Sir:

The attached sheets contain the Rule 41.37 items of appellant's Appeal Brief. The Director is hereby authorized to charge the fee for filing a brief in support of the appeal plus any other necessary fees to the deposit account of Texas Instruments Incorporated, account No. 20-0668.

Respectfully submitted,

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Rule 41.37(c)(1)(i) Real party of interest

Texas Instruments Incorporated owns the application.

Rule 41.37(c)(1)(ii) Related appeals and interferences

There are no related dispositive appeals or interferences.

Rule 41.37(c)(1)(iii) Status of claims

Pursuant to MPEP 1205.02, for each claim in the case appellant states the status as follows:

Claim 1: cancelled

Claim 2: rejected

Claim 3: rejected

Claim 4: rejected

Claim 5: rejected

Claim 6: rejected

Claim 7: rejected

Claim 8: rejected

Claim 9: rejected

Claim 10: rejected

Claim 11: rejected

Claim 12: rejected

Claim 13: rejected

Claim 14: rejected

Claim 15: rejected

Claim 16: rejected

Claim 17: rejected

Claim 18: rejected

Claim 19: rejected

Claim 20: rejected

Claim 21: rejected

Claim 22: rejected

Claim 23: rejected

Claim 24: cancelled

Claim 25: rejected

Claim 26: rejected

Pursuant to MPEP 1205.02, appellant identifies each claim on appeal as follows

Claim 2: on appeal

Claim 3: on appeal

Claim 4: on appeal

Claim 5: on appeal

Claim 6: on appeal

Claim 7: on appeal

Claim 8: on appeal

Claim 9: on appeal

Claim 10: on appeal

Claim 11: on appeal

Claim 12: on appeal

Claim 13: on appeal

Claim 14: on appeal

Claim 15: on appeal

Claim 16: on appeal

Claim 17: on appeal

Claim 18: on appeal

Claim 19: on appeal

Claim 20: on appeal

Claim 21: on appeal

Claim 22: on appeal

Claim 23: on appeal

Claim 25: on appeal

Claim 26: on appeal

Rule 41.37(c)(1)(iv) Status of amendments

There is no amendment after final rejection.

Rule 41.37(c)(1)(v) Summary of claimed subject matter

The independent claims on appeal consist of device claim 2, system claim 12, method claim 25, and method claim 26.

The subject matter of claim 2 is an integrator circuit (application page 10, lines 2-8; FIG.3 item 30) comprising an input conductor for conducting an input current (application page 3, lines 10-11; page 10, lines 2-8; FIG.3, item Iin); a first amplifier stage having an input coupled to the input conductor (application page 3, lines 10-12; page 10, lines 2-8; FIG.3, item 11); a second amplifier stage having an output and also having an input coupled to an output of the first amplifier stage (application page 3, lines 12-14; page 10, lines 2-8; FIG.3, item 13); an integrating capacitor coupled between the input of the first amplifier stage and the output of the second amplifier stage (application page 3, lines 16-17; page 10, lines 2-8; FIG.3, item C_{INT}); and an MOS compensation capacitor coupled between the input and output of the second amplifier stage (application page 10, lines 2-8; FIG.3, item 20 (C_C)).

The subject matter of claim 12 is a CT scanner data acquisition system (application page 1, line 10 through page 2, line 16; FIGS.1-2) comprising a plurality of integrator circuits (application page 2, line 7; FIG.2 items 2A-1, 2A-2, 2B-1, 2B-2), each including (i) an input conductor for conducting an input current (application page 3, lines 10-11; page 10, lines 2-8; FIG.3, item Iin), (ii) a first amplifier stage having an input coupled to the input conductor (application page 3, lines 10-12; page 10, lines 2-8; FIG.3, item 11), (iii) a second amplifier stage having an output and also having an input coupled to an output of the first amplifier stage (application page 3, lines 12-14; page 10, lines 2-8; FIG.3, item 13), (iv) an integrating capacitor coupled between the input of the first amplifier stage and the output of the second amplifier stage (application page 3, lines 16-17; page 10, lines 2-8; FIG.3, item C_{INT}), and (v) an MOS compensation capacitor coupled between the input and output of the second amplifier stage (application

page 10, lines 2-8; FIG.3, item 20 (C_C)), a plurality of photodiodes each having an anode coupled to an input conductor of an integrator circuit, respectively (application page 2, lines 4-5, 19; page 3, lines 1-5; FIG.1 items D-1, ..., D-(N-1)); a plurality of analog-to-digital converters, inputs of the analog-to-digital converters being coupled to the outputs of various integrator circuits (application page 3, line 6; FIGs.1-2 item 15).

The subject matter of claim 25 is a method of operating an integrator circuit, comprising conducting an input current into an input conductor of a first amplifier stage (application page 3, lines 10-11; page 10, lines 2-8; FIG.3, item Iin); coupling an input of a second amplifier stage to an output of the first amplifier stage (application page 3, lines 12-14; page 10, lines 2-8; FIG.3, item 13), charging an integrating capacitor coupled between the input of the first amplifier stage and an output of the second amplifier stage (application page 3, lines 16-17; page 10, lines 2-8; FIG.3, item C_{INT}); and compensating the integrator circuit by controlling the bandwidth of the integrator circuit by biasing an MOS compensation capacitor coupled between the input and output of the second amplifier stage into a predetermined operating region range (application page 10, lines 2-8; page 12, lines 4-10; FIG.3, item 20 (C_C)).

The subject matter of claim 26 is a method of operating a CT scanner data acquisition system (application page 1, line 10 through page 2, line 16; FIGS.1-2), comprising in each of a plurality of integrator circuits (application page 2, line 7; FIG.2 items 2A-1, 2A-2, 2B-1, 2B-2), (i) conducting an input current into an input conductor of a first amplifier stage (application page 3, lines 10-11; page 10, lines 2-8; FIG.3, items Iin and 11), (ii) coupling an input of a second amplifier stage to an output of the first amplifier stage (application page 3, lines 10-14; page 10, lines 2-8; FIG.3, items 11, 13), (iii) charging an integrating capacitor coupled between the input of the first amplifier stage and an output of the second amplifier stage (application page 3, lines 16-17; page 10, lines 2-8; FIG.3, item C_{INT}); and (iv) compensating the integrator circuit by controlling the bandwidth of the integrator circuit by biasing an MOS compensation capacitor coupled between the input and output of the second amplifier stage into a predetermined

operating region range (application page 10, lines 2-8; page 12, lines 4-10; FIG.3, item 20 (C_C)); coupling an anode of each of a plurality of photodiodes to an input conductor of a group of integrator circuits, respectively (application page 2, lines 4-5, 19; page 3, lines 1-5; FIG.1 items D-1, ..., D-(N-1), D-N and 10-1, 10-2, ..., 10-(N-1), 10-N); and coupling inputs of a plurality of analog-to-digital converters to the outputs of various groups of integrator circuits, respectively (application page 3, line 6; FIGS.1-2 items 14 and 15).

Rule 41.37(c)(1)(vi) Grounds of rejection to be reviewed on appeal

The grounds of rejection to be reviewed on appeal are:

1. Claims 2-23 and 25-26 were rejected under 35 USC § 103(a) as unpatentable over the prior art depicted by Applicant's Figs. 1-2 and further in view of Verhaeghe et al (USP 5,479,132) or Rapp (USP 5,280,420) or Jung (US 2005/0127885).

Rule 41.37(c)(1)(vii) Arguments

1. Claims 2-23 and 25-26 were rejected under 35 USC § 103(a) as unpatentable over the prior art depicted by Applicant's Figs. 1-2 and further in view of Verhaeghe or Rapp or Jung.

Claims 2-11: Applicant's prior art Fig.2 shows integrator circuits 2A-1 and 2A-2 with two amplfiier stages plus feedback integrating capacitor C_{INT} and feedback compensation capacitor C_C with both capacitors as polysilicon capacitors. In contrast, claim 2 requires a two-amplifier-stage integrator with a feedback integrating capacitor plus a MOS feedback compensation capacitor; and Fig.2 does not suggest a MOS capacitor because MOS capacitors have a non-linear voltage dependent capacitance (e.g., application FIG.5) and are noisy. Further, the feedback integrating capacitor needs to avoid voltage-dependent capacitance for linearity of the integrator (e.g., application page 11, line 19 to page 12, line 3), so the feedback integrating capacitor cannot be a MOS capacitor and thus the feedback compensation capacitor in the same circuit would also not be a MOS capacitor.

Thus, the Examiner cited MOS capacitors of Verhaeghe, Rapp, and Jung as making obvious the substitution of a MOS capacitor for the feedback compensation polysilicon capacitor in applicant's prior art Fig.2. However, Verhaeghe's capacitor 14 in Fig.1 is not a feedback compensation capacitor in a two-amplifier-stage integrator as claimed, but it is part of an RC integration circuit. This does not suggest anything about an amplfier compensation capacitor. Furthermore, Verhaighe Fig.4A replaces capacitor 14 with a combination of NMOS capacitor 40 plus PMOS capacitor 42 because of the problem of voltage dependent capacitance of the MOS capacitors; see column 3, lines 24-29. That is, Verhaeghe does not suggest anything about the feedback compensation capacitor of the two-amplifier-stage integrator of claim 2 plus avoids a simple substitution with a single MOS capacitor due to the voltage-dependence of the capacitance.

Similarly, cited column 7, lines 10-16 of Rapp relate to capacitors in charge pumps 42 and 46 (Rapp Fig.3) which do not need to avoid voltage dependent capacitance and do not suggest anything about the capacitors of the two-amplfier-stage integrator of claim 2.

Likewise, Jung Fig.3 refers to capacitor 112 of Fig.2 in a voltage regulator and does not suggest anything about the capacitors of the two-amplifier-stage integrator of claim 2.

Claims 12-23: Claim 12 is a CT scanner with photodiode output signal integrators where the integrators are as in claim 2; and so the foregoing arguments about a MOS compensation capacitor together with the feedback integrating capacitor in a two-amplifier-stage integrator apply.

Indeed, applicant's invention includes the realization that the non-linear noise character of the CT scanner photodiode output signals allows for the claimed use of non-linear feedback compensation capacitors in the integrators leading to tolerable non-linear integrator noise; see application Fig.6.

Claim 25: Claim 25 is a method of operating the integrator of claim 2, and the foregoing arguments about using a MOS compensation capacitor together with the feedback integrating capacitor in a two-amplifier-stage integrator apply.

Claim 26: Claim 26 is a method of operating the CT scanner of claim 12, and the foregoing arguments about using a MOS compensation capacitor together with the feedback integrating capacitor in a two-amplifier-stage integrator in the photodiode output signal integrator apply.

Rule 41.37(c)(1)(viii) Claims appendix

Claim 2 (original) An integrator circuit comprising:

(a) an input conductor for conducting an input current;

(b) a first amplifier stage having an input coupled to the input conductor ;

(c) a second amplifier stage having an output and also having an input coupled to an output of the first amplifier stage;

(d) an integrating capacitor coupled between the input of the first amplifier stage and the output of the second amplifier stage; and

(e) an MOS compensation capacitor coupled between the input and output of the second amplifier stage.

Claim 3 (original) The integrator circuit of claim 2 wherein the first amplifier stage includes an input stage having an output coupled to an input of a folded cascode stage, an output of the folded cascode stage being coupled to a first terminal of the MOS capacitor, a second terminal of the MOS capacitor being coupled to the output of the second amplifier stage.

Claim 4 (original) The integrator circuit of claim 3 wherein the first and second amplifier stages co-act to establish bias voltage across the MOS capacitor so as to bias the MOS capacitor in its accumulation region for low values of the input current to provide a high value of compensation capacitance for the integrator circuit and so as to bias the MOS capacitor in its inversion region for high values

of the input current to provide a low value of compensation capacitance for the integrator circuit.

Claim 5 (original) The integrator circuit of claim 4 wherein the input current is a photodiode current containing a relatively low amount of noise for the low values of the input current and containing a higher amount of noise for the high values of the input current, and wherein an amount of noise produced by the integrator circuit when the value of the compensation capacitance is high is masked by the relatively high amount of noise.

Claim 6 (original) The integrator circuit of claim 2 wherein the first amplifier stage is a non-inverting amplifier stage and the second amplifier stage is an inverting amplifier stage.

Claim 7 (original) The integrator circuit of claim 2 wherein the MOS compensation capacitor includes an N-channel source region and an N-channel drain region both coupled to the input of the second stage amplifier, and also includes a gate disposed over a channel region between the N-channel source region and the N-channel drain region, the gate being coupled to the output of the second amplifier stage.

Claim 8 (original) The integrator circuit of claim 7 wherein the integrating capacitor is a poly capacitor.

Claim 9 (original) The integrator circuit of claim 2 wherein the input of the first amplifier stage conducts a single-ended input signal.

Claim 10 (original) The integrator circuit of claim 2 wherein the input of the first amplifier stage conducts a differential input signal.

Claim 11 (original) The integrator circuit of claim 6 wherein the second stage amplifier is an inverting class A amplifier.

Claim 12 (original) A CT scanner data acquisition system comprising:

(a) a plurality of integrator circuits, each including

i. an input conductor for conducting an input current,

ii. a first amplifier stage having an input coupled to the input conductor,

iii. a second amplifier stage having an output and also having an input coupled to an output of the first amplifier stage,

iv. an integrating capacitor coupled between the input of the first amplifier stage and the output of the second amplifier stage, and

v. an MOS compensation capacitor coupled between the input and output of the second amplifier stage;

(b) a plurality of photodiodes each having an anode coupled to an input conductor of an integrator circuit, respectively;

(c) a plurality of analog-to-digital converters, inputs of the analog-to-digital converters being coupled to the outputs of various integrator circuits.

Claim 13 (original) The CT scanner data acquisition system of claim 12 wherein the first amplifier stage includes an input stage having an output coupled to an input of a folded cascode stage, an output of the folded cascode stage being coupled to a first terminal of the MOS capacitor, a second terminal of the MOS capacitor being coupled to the output of the second amplifier stage.

Claim 14 (original) The CT scanner data acquisition system of claim 13 wherein the second amplifier stages co-act to establish bias voltage across the MOS capacitor so as to bias the MOS capacitor in its accumulation region for low values of the input current to provide a high value of compensation capacitance for the integrator circuit and so as to bias the MOS capacitor in its inversion region for high values of the input current to provide a low value of compensation capacitance for the integrator circuit.

Claim 15 (original) The integrator circuit of claim 14 wherein the input current is a photodiode current containing a relatively low amount of noise for the low values of the input current and containing a relatively high amount of noise for the high values of the input current, wherein an amount of noise produced by the integrator circuit when the value of the compensation capacitance is high is masked by the relatively high amount of noise.

Claim 16 (original) The CT scanner data acquisition system of claim 12 wherein the analog-to-digital converters are delta-sigma analog-to-digital converters.

Claim 17 (original) The CT scanner data acquisition system of claim 12 wherein the inputs of the analog-to-digital converters are coupled to common outputs of groups of the integrator circuits, respectively.

Claim 18 (original) The CT scanner data acquisition system of claim 12 wherein the first amplifier stage is an operational amplifier stage and the second amplifier stage is an inverting amplifier stage.

Claim 19 (original) The CT scanner data acquisition system of claim 12 wherein the MOS compensation capacitor includes an N-channel source region and an N-channel drain region both coupled to the input of the second stage amplifier, and also includes a gate disposed over a channel region between the N-channel source region and the N-channel drain region, the gate being coupled to the output of the second amplifier stage.

Claim 20 (original) The CT scanner data acquisition system of claim of 19 wherein the integrating capacitor is a poly capacitor.

Claim 21 (original) The CT scanner data acquisition system of claim 12 wherein the input of the first amplifier stage conducts a single-ended input signal.

Claim 22 (original) The CT scanner data acquisition system of claim 12 wherein the input of the first amplifier stage conducts a differential input signal.

Claim 23 (original) The CT scanner data acquisition system of claim 12 wherein the second stage amplifier is an inverting class A amplifier.

Claim 25 (original) A method of operating an integrator circuit, comprising:

(a) conducting an input current into an input conductor of a first amplifier stage;

(b) coupling an input of a second amplifier stage to an output of the first amplifier stage;

(c) charging an integrating capacitor coupled between the input of the first amplifier stage and an output of the second amplifier stage; and

(e) compensating the integrator circuit by controlling the bandwidth of the integrator circuit by biasing an MOS compensation capacitor coupled between the input and output of the second amplifier stage into a predetermined operating region range.

Claim 26 (original) A method of operating a CT scanner data acquisition system, comprising:

(a) in each of a plurality of integrator circuits,

i. conducting an input current into an input conductor of a first amplifier stage,

ii. coupling an input of a second amplifier stage to an output of the first amplifier stage,

iii. charging an integrating capacitor coupled between the input of the first amplifier stage and an output of the second amplifier stage; and

iv. compensating the integrator circuit by controlling the bandwidth of the integrator circuit by biasing an MOS compensation capacitor coupled between the input and output of the second amplifier stage into a predetermined operating region range;

(b) coupling an anode of each of a plurality of photodiodes to an input conductor of a group of integrator circuits, respectively;

(c) coupling inputs of a plurality of analog-to-digital converters to the outputs of various groups of integrator circuits, respectively.

Rule 41.37(c)(1)(ix) Evidence appendix

none

Rule 41.37(c)(1)(x) Related proceedings appendix

none